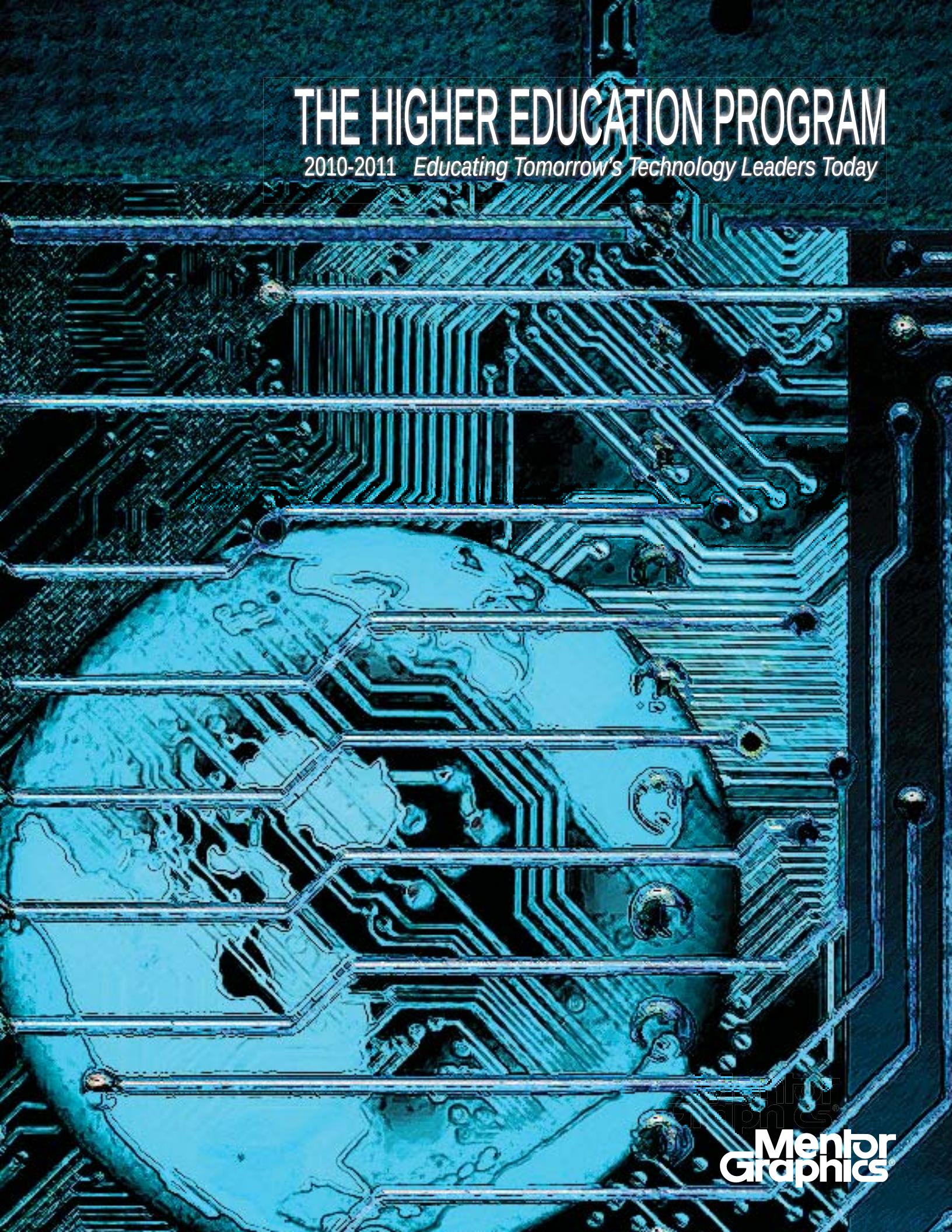
THE HIGHER EDUCATION PROGRAM

2010-2011 *Educating Tomorrow's Technology Leaders Today*



Mentor Graphics®

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INTRODUCTION

Welcome to Mentor Graphics' Higher Education Program (HEP).

Mentor Graphics, a technology leader in electronic design automation (EDA) with the broadest industry portfolio of best-in-class products, founded the Higher Education Program (HEP) in 1985 to further the development of skilled engineers within the electronics industry. HEP provides schools around the globe with leading edge design tools for classroom instruction and academic research to help ensure that engineering graduates enter industry proficient in state-of-the-art tools and techniques. To date, Mentor Graphics is proud to have partnered with more than 1200 academic institutions worldwide.

In this brochure you will find details on the Mentor Graphics products available through HEP. We organize our products into a series of design packages from which you will choose based on your EDA needs. Upon admittance to the program, you will receive licenses and media for all products in the package(s) that you choose. This ensures that you receive the maximum benefit for each package's support charge and that you receive your desired products and all optional components immediately, without the need to request changes to your configuration mid-term.

For our existing members, please make sure that you check Renewing Members Only Section; each year strategic decisions are made that may necessitate adding and/or removing products from the program. To apply for or renew your annual HEP membership, please visit www.mentor.com/company/higher_ed/.

Thank you once again for your continued support. We hope you have a productive year as a member of Mentor Graphics Higher Education Program!

Sincerely,

HEP Development Director
Mentor Graphics

TABLE OF CONTENTS

PRODUCT PACKAGES

For 2010-11, Mentor Graphics products available through HEP are divided into eight (8) product packages. Table 1 shows these packages and their corresponding support prices. When you order your HEP software you will select by package, and you will receive licenses and media for all products included in that package. (Support Fees are irrespective of the number of licenses you require.)

DESCRIPTION	MAIN PRODUCT COMPONENTS	US SUPPORT PRICE
IC Nanometer Design	ADiT™, Eldo®, ADVance MS™, CommLib™, Design Architect®-IC, IC Station®, Calibre®	$500
Design, Verification & Test	ModelSim®, Questa™ AFV, FPGA Advantage®, Precision™ Synthesis, Leonardo Spectrum™, Tessent™ Silicon Test, Seamless® Co-Verification, SystemVision™ System Modeling, Bridgepoint®, O-In®, Summit	$500
PCB Expedition	Expedition Design Capture, Expedition Pinnacle™ Layout, I/O Designer™ FPGA Integration, Tau® Timing Analysis, Fablink™ XE Pro, HyperLynx® GHz, Quiet™ Expert , Eldo, DxDesigner™	$200
PCB PADS	PADS Logic, PADS Layout, PADS Autorouter Eldo, HyperLynx® GHz	$500
Embedded SW Development	Nucleus® EDGE™, Nucleus Profiler & Debugger C/C++ Compiler Tools, GNU Compiler Tools, Nucleus SIMdx	$500
Cabling & Harness	Capital Design, Views, Analyisis and Harness; SystemVision	$500
Vehicle Networking	Volcano Network Architect, Volcano LIN Network Architect, SystemVision	$500
Mechanical Analysis	FloTHERM™, FloTHERM PCB, FloTHERM PACK FloVENT™, FloEFD™, FloEFD Electronic Cooling & Adv CFD	$500
PCB BoardStation	This package is only available as a renewal.	$500

**For international pricing and product options, please contact your regional HEP representative.

ASIC DESIGN KIT

The ASIC Design Kit (ADK) is a generic design kit providing all the requisite data, libraries, and documentation to create ASIC designs using the Mentor suite of layout, synthesis, simulation, and DFT tools. Its primary use is by universities and colleges in classroom environments. The target technologies are AMI 0.5m and 1.2m and TSMC 0.35m, 0.25m and 0.18m.

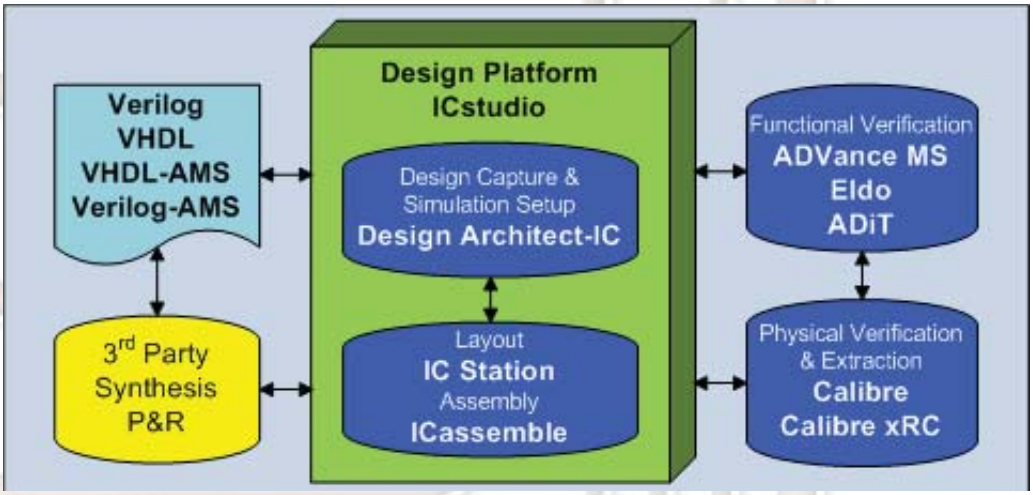
The kit provides:

- Support for schematic, HDL or mixed schematic/HDL based designs
- Synthesis support for Leonardo Spectrum
- Pre-layout timing simulations with QuickSim and ModelSim (VHDL or Verilog)
- Design for Test
- Static timing analysis models for SST Velocity
- Automatic place and route of designs using IC Station
- Post-layout timing simulations with QuickSim, ModelSim (VHDL/Verilog), Mach TA, or Eldo

The latest version of the ASIC Design Kit is ADK 3.1. This version supports all appropriate tools in HEP. For further information, to register and download the ADK, please visit the IC and ASIC Design Kits website.

IC NANOMETER DESIGN

The IC Nanometer Design package provides a complete environment for the design, capture, layout and verification of analog, digital and mixed-signal integrated circuits.



Package 1 includes all products that incorporate the IC Nanometer Design platform:

- Design Architect-IC - A powerful tool for schematic capture, netlisting, simulation setup and results viewing.
- IC Station - Provides the physical layout component of the Mentor Graphics full custom IC design flow. This suite includes application bundles for editing, schematic-driven layout, and top-level floor planning/ routing.
- ICassemble - A robust set of features for floor planning, top-level assembly and interactive routing.
- ADVance MS and ADVance MS RF - A language-neutral, mixed-signal simulator that enables top-down design and bottom-up verification of multi-million gate analog/mixed-signal SoC designs.
- Eldo and Eldo RF - An analog simulator offering numerous simulation and modeling options that deliver high-performance and high-speed simulation with the accuracy required by the user.
- ADiT™ - A fast-SPICE simulator built specifically for analog and mixed-signal applications.
- Calibre - The industry standard platform for physical verification, offering superior performance and capacity for both flat and hierarchical algorithms.
- Calibre xRC - Accurate transistor-level, gate-level and hierarchical parasitic extraction.

IC NANOMETER DESIGN TOOLS

ANALOG-MIXED SIGNAL IC SIMULATION

AVAILABLE PLATFORMS: Linux SUN

227863	ADiT TURBO Ap SW
242925	Questa ADMS Dual Lang Bnd SW
212235	Questa ADMS RF Op SW
130007	Artist Link Ap SW
204979	Eldo RF Op SW
237473	ADiT Rail Op SW
51630	HDL-A/DEV V8 Op SW

IC-FLOW

AVAILABLE PLATFORMS: Linux SUN

233852	ICanalyst CC Ap SW
233853	ICanalyst CB Ap SW
217713	IC Station Schematic Ap SW
221498	IC EDIF200 Netlist Read Stn SW
221494	IC EDIF200 Sch Reader Bnd SW
221496	IC EDIF200 Sch Writer Stn SW
221499	IC EDIF300/400 Netlist Read Stn SW
221500	IC EDIF300/400 Netlist Write Stn SW
221495	IC EDIF300/400 Sch Read Bnd SW
221497	IC EDIF300/400 Sch Write Stn SW
212040	IC Station Layout Gen Bnd SW
210433	ICassemble Op SW
63084	IC Station Layout Ap SW
54769	Schematic Generator V8 Ap SW
44110	AutoCells Ap SW
54743	Back Annotation Op SW
54744	Clock Tree Op SW
30000	Falcon Framework V8 Ap SW
51688	HotPlot HP-RTL Ap SW
34689	ICrules Op SW
34691	ICtrace Op SW
34641	IC Station Layout SDL

PHYSICAL VERIFICATION & EXTRACTION

AVAILABLE PLATFORMS: Linux SUN

212210	Calibre PVS Stn SW
	Calibre nmDRC Ap SW
	Calibre nmDRC-H Op SW
	Calibre Interactive Ap SW
	Calibre RVE/QDB-H Ap SW
	Calibre nmLVS Ap SW
	Calibre nmLVS-H Op SW

PHYSICAL VERIFICATION & EXTRACTION

AVAILABLE PLATFORMS: Linux SUN

210681	Calibre DESIGNrev Ap SW
226095	Calibre FRACTUREc Op SW
220546	Calibre FRACTUREh Op SW
211030	Calibre FRACTUREj Op SW
209427	Calibre FRACTUREm Op SW
212329	Calibre FRACTUREt Op SW
231209	Calibre FRACTUREv Op SW
207041	Calibre LITHOview Ap SW
224372	Calibre MDP Embedded SVRF Op SW
220547	Calibre MDPmerge Op SW
210899	Calibre MDPview Ap SW
224371	Calibre MPCPro Op SW
205003	Calibre MT-2nd CPU Op SW
205564	Calibre MT-OPCpro Op SW
231422	Calibre nmOPC Op SW
204413	Calibre OPCpro Op SW
211566	Calibre OPCsbar Op SW
225747	Calibre OPCverify Op SW
203329	Calibre ORC Op SW
204415	Calibre PSMgate Op SW
211565	Calibre TDopc Op SW
204416	Calibre WORKbench Ap SW
221191	Calibre xL Op SW
210228	Calibre xRC Ap SW
234967	Calibre YieldAnalyzer Bnd SW
234968	Calibre YieldEnhancer Bnd SW
226492	Calibre LFD Ap SW
226494	Calibre MTLFD Op SW
208309	Calibre CB Ap SW
218002	Calibre xRC CB Ap SW
223993	Calibre ADP Op SW
225771	Calibre ILO Op SW
231096	Calibre YieldServer Ap SW
233752	Calibre CMPAnalyzer Op SW
235012	Calibre MASKOPT Op SW
235811	Calibre PERC Ap SW
237747	Calibre nmMPC Op SW
238686	Calibre FRACTUREall Op SW
240233	Calibre nmDP-C Op SW
231210	Calibre MetrologyAPI Op SW-LSL3
223155	Time-it Op SW
67851	xCalibrate Ap SW

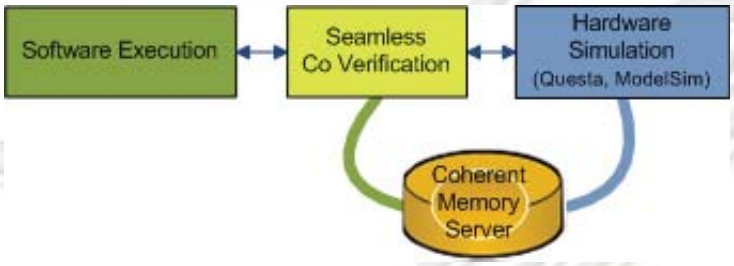
DESIGN, VERIFICATION & TEST

HEP's Design, Verification and Test package provides complete solutions for HDL design, verification, synthesis and test of ASICs and FPGAs:

- Questa Advanced Functional Verification Platform – Completely standards based, Questa is the most advanced functional verification product in the industry, supporting assertion based verification, coverage driven verification, testbench automation and formal analysis of clock domain crossing, supported by a comprehensive suite of Verification IP.
- inFact – A testbench automation toolset that enables designers and verification engineers to achieve higher coverage in less time when used with Questa, ModelSim, or other simulators. Unlike writing directed tests, inFact automatically generates testbench sequences for simulation. And, unlike random tests, inFact does not require algebraic constraints to prevent the generation of illegal sequences.
- FPGA Design and Verification – A complete solution comprising HDL design, simulation, hardware-software co-verification and leading FPGA logic and physical synthesis.
- C Based Design and Verification – A comprehensive suite of tools for design creation and analysis using C and System C.
- Tessent Silicon Test – A complete technology-leading solution for testability analysis, scan, boundary scan and memory test synthesis, and automatic test pattern generation.
- Hardware-Software Co-Verification – The industry's leading solution for verification of hardware and software.
- System Modeling – A complete environment for creation and verification of mixed-signal and multi-language systems, prevalent in automotive electrical systems, control systems and mechatronic systems.

HARDWARE/SOFTWARE CO-VERIFICATION

Mentor Graphics' Seamless Co-Verification Environment provides for the verification of both hardware and software in an embedded system. Seamless allows for a virtual prototype instead of having to build a physical prototype. Early debug reduces risk of having to re-design the system.



Seamless is available as two products:

- Seamless - Co-verification environment that detects and isolates hardware/software interface errors.
- Seamless FPGA - Co-verification environment that detects and isolates hardware/software interface errors for Platform FPGAs. Seamless FPGA provides a single button, automated Seamless setup, and includes the PowerPC 405 Processor Support Package for the Xilinx Virtex-II technology.

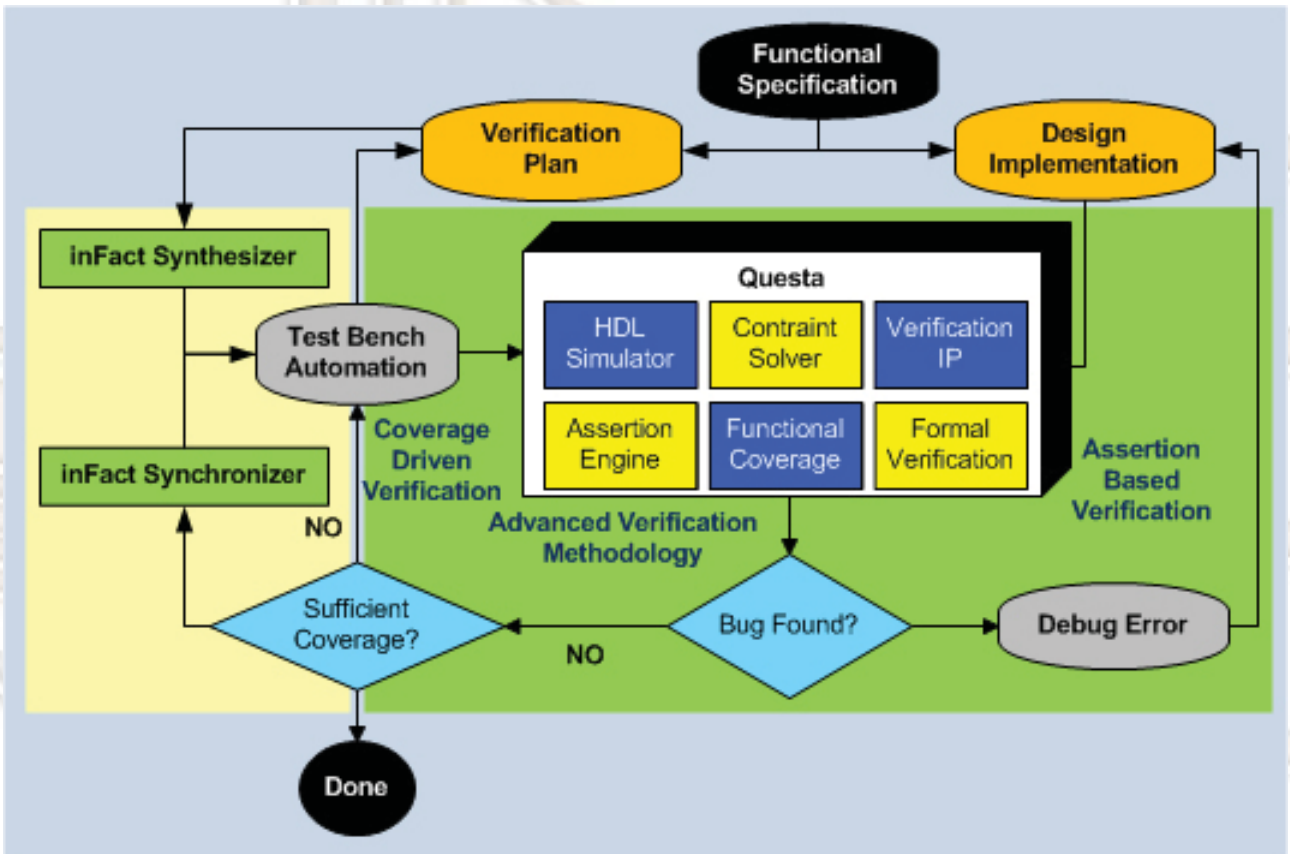
DESIGN, VERIFICATION & TEST

QUESTA/0-In ADVANCED FUNCTIONAL VERIFICATION

Questa is Mentor Graphics' Advanced Verification Environment and is the only integrated verification platform that can improve quality, productivity, and predictability for any verification flow.

Benefits:

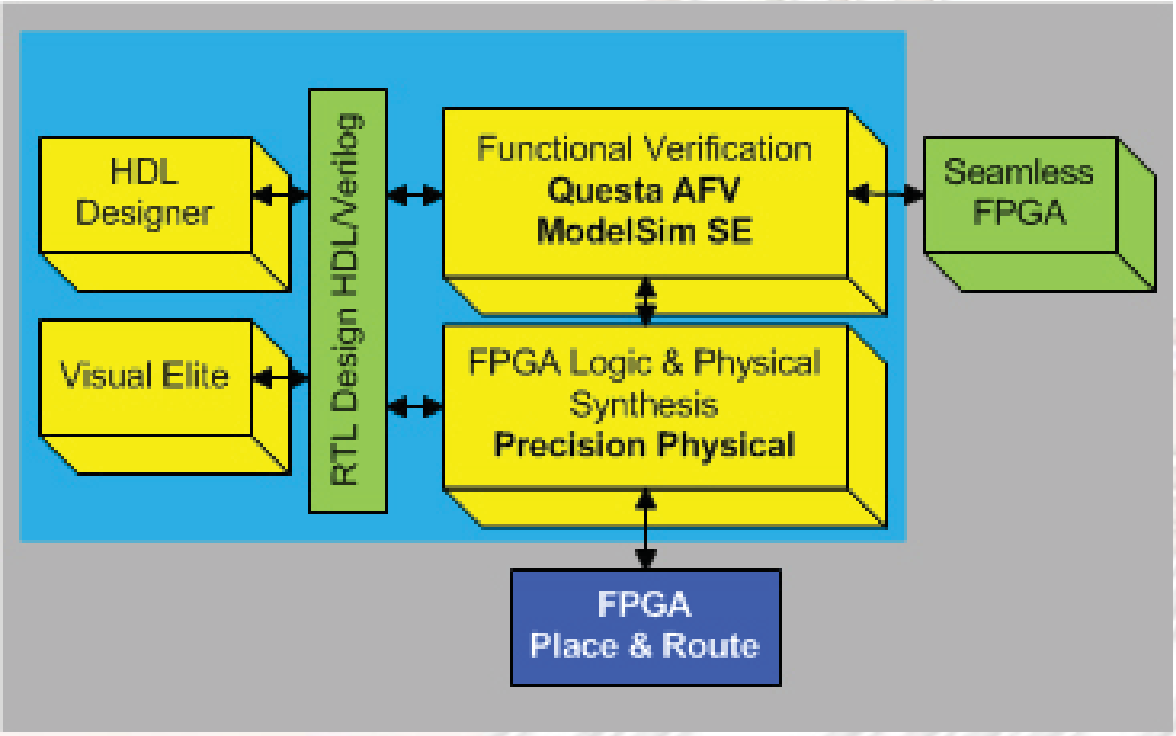
- Standards-based solution to support all flows, secure your verification investment, and enable interoperability.
- High-performance solution built on the best-in-class ModelSim simulator supporting all standard languages, VHDL, Verilog, SystemVerilog, Verilog, SystemC, and PSL.
- Industry leading Clock Domain Crossing (CDC) verification to find the most critical, hard-to-find bugs.
- Assertion Based Verification using both SystemVerilog and PSL for improving quality.
- Coverage Driven Verification and testbench automation for improving productivity and design quality.
- Formal Verification allows improvement of overall verification quality and finds the most critical bugs in your design.



FPGA DESIGN & VERIFICATION

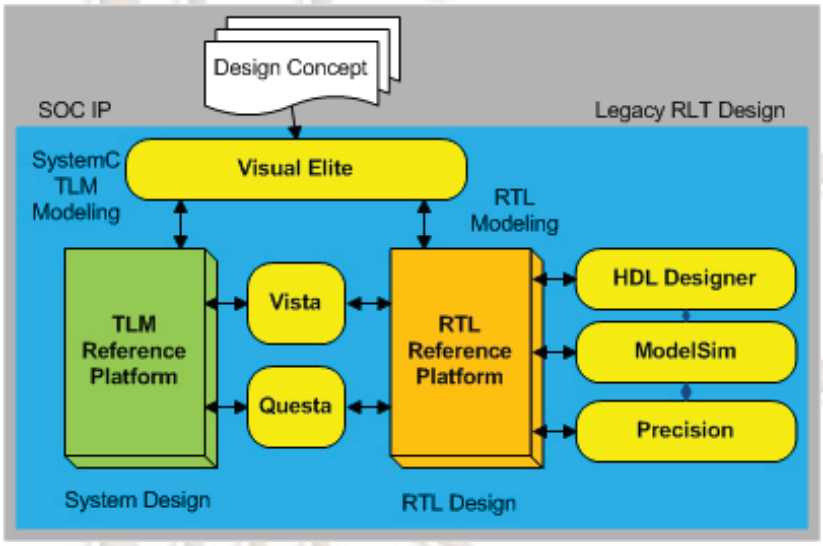
Mentor Graphics supports a complete flow for the design and verification of complex FPGAs and field programmable SOCs.

- HDL Designer™ – A graphical HDL design environment that enables scalable RTL design, spanning FPGAs to multimillion gate ASICs; creates and manages complex Verilog, VHDL, and mixed-language ASIC and FPGA designs.
- Visual Elite™ - A state-of-the-art design and integration platform enabling designers and system architects to intuitively capture and connect SystemC and HDL blocks into complex SoCs and systems.
- ModelSim SE™ – The industry's most widely used verification environment. ModelSim's single kernel architecture supports all standard languages including VHDL, Verilog & SystemC.
- Precision® RTL Plus – Delivers outstanding quality of results for FPGA synthesis from VHDL & Verilog. An integrated RTL and physical FPGA synthesis solution, built on a single data model, simultaneously optimizes gate and interconnect delay.
- Seamless FPGA – Verification of hardware & software in an embedded system, Seamless FPGA provides a single button, automated set up for FPGA verification.



DESIGN, VERIFICATION & TEST

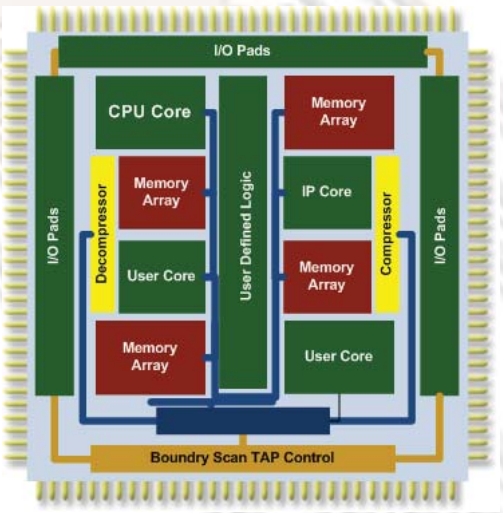
ELECTRONIC SYSTEM LEVEL DESIGN



- Visual Elite™ - A state-of-the-art design and integration platform enabling designers and system architects to intuitively capture and connect SystemC and HDL blocks into complex SoCs and systems.
- Vista™ - A state-of-the-art source-based SystemC debug toolset, providing powerful hardware and C/C++ oriented views and debugging mechanisms.
- System Architect ™ - Provides a unique modeling and analysis toolset for creating cycle-accurate TLM performance and power models along with higher-level, more abstract token-based models.

SILICON TEST

Mentor Graphics' Tessent™ Silicon Test products a complete solution for achieving high test quality, low test cost for the whole chip.



The Tessent product family includes:

Scan ATPG and Compression
- Tessent FastScan™: Direct Scan test
- Tessent SoCScan: Complete scan insertion

Memory Test
- Tessent MemoryBIST: Built-in Self Test
- Tessent FastScan MacroTest

Boundary Scan
- Tessent BoundaryScan: IEEE 1149.1 compliant board test

DESIGN, VERIFICATION & TEST TOOLS

DESIGN, ENTRY & SYNTHESIS		AVAILABLE PLATFORMS
207964	HDL Designer Ap SW	
238001	HDL Designer IP-XACT Ap SW	
211639	Precision RTL Synthesis Ap SW	
233858	Precision RTL Plus Ap SW	Linux, SUN, WIN
204437	Spectrum Lev 3 ASIC-VHDL Ap SW	
204436	Spectrum Lev 3 ASIC-VLOG Ap SW	
204435	Leonardo Insight Op SW	
204434	Leo Spectrum Lev 3-ASIC Op SW	
204439	XLIB Creator Ap SW	WIN
236144	Vista Architect Stn SW	
232656	Visual SLD Pro Stn SW-MD	
239154	Visual SLD Pro LNL Plus Stn SW	Linux, SUN, WIN
237015	Certe Testbench Studio Ap SW	
237476	Certe TB for HDL Des Op SW	
235911	HDL Des-Visual Com Lic Ap SW	
239732	Vista HCE Op SW	

FUNCTIONAL VERIFICATION		
205146	ModelSim SE MixedHDL Ap SW	
219261	SystemC Op SW	
222421	Profiler Op SW	
224747	Questa AFV Ap SW	
241221	Codelink HVE Inspector Op SW	Linux, SUN, WIN
241222	Codelink HVE Tracer Ap SW	
237965	CW Compiler Ap SW	
243168	CDC Ap SW	
243169	Formal Ap SW	
222972	FX Eng Op SW	
235831	Questa MVC Library Op SW	

CED PRODUCTS		
204610	FormalPro V8 Ap SW	SUN, LNX
054769	Schematic Generator V8 Ap SW	

DESIGN-FOR-TEST		AVAILABLE PLATFORMS
242156	Tessent MemoryBIST Ap SW	
242160	Tessent BoundaryScan Ap SW	
242174	Tessent SoCScan Ap SW	Linux, SUN
43879	Tessent FastScan Ap SW	
202287	Tessent FastScan MacroTest Op SW	

SLE PRODUCTS		
204591	Seamless CVE no Denali Ap SW	
212985	Seamless FPGA-Xilinx Ap SW	Linux, SUN
228131	Freescale Family Op SW	
236643	inFact AFV Ap SW	Linux, SUN
230522	BridgePoint UML Suite C Ap SW	WIN
235832	BridgePoint MC Exec C Op SW	

SYSTEMVISION PRODUCTS		
238218	SystemVision 650 Bnd SW	WIN

PCB TOOLS

Mentor Graphics is the market leader in PCB design, implementation & analysis. Our integrated solutions support a complete flow for design definition with schematics & HDL, FPGA integration for reduced design cycles, an integrated layout & routing environment & powerful signal integrity analysis tools.

For HEP's new members, Mentor Graphics has two product offerings in the area of printed circuit board design. These are Expedition– the most powerful solution targeted at the mid-sized to large organization or for the systems design group with pervasive use of leading edge PCB or high speed technologies and PADS– a complete PCB design solution combining schematic definition with powerful layout & simulation tools.

Included in each of these product lines is HyperLynx, Mentor's powerful signal and power integrity analysis suite. The HyperLynx suite of tools can be used in virtually any design flow to help eliminate signal integrity, crosstalk, & EMC problems early, allowing you to "get it right the first time." These simulation tools come ready to use with unprecedented ease of use, delivering high-speed analysis to every engineer's desktop.

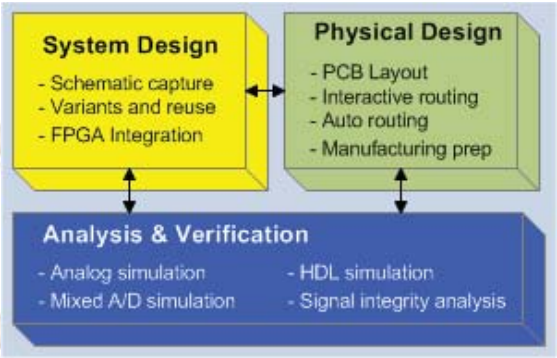
For PCB products that may be available to renewing HEP members, please visit the supplemental brochure.

PCB PADS

PADS is a complete PCB design solution combining schematic definition with powerful layout & simulation tools. It provides an integrated design environment combining ease of use with functional depth.

With PADS PCB design solutions, you will:

- Achieve a high ROI on PCB designs ranging from basic to complex.
- Improve productivity with shorter design cycles.
- Maintain design integrity with the latest analysis and simulation tools.



PCB PADS TOOLS

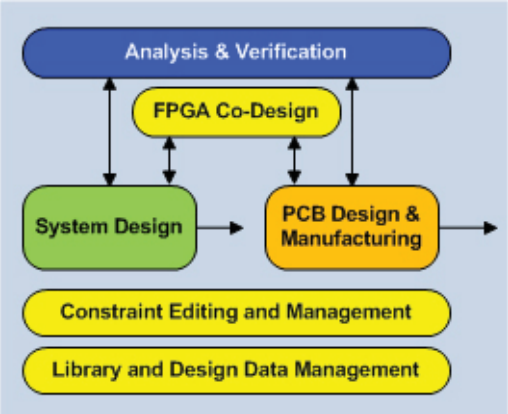
PCB DESIGN		AVAILABLE PLATFORMS
240146	DxDesigner 040 Ap SW	WIN
237180	PADS Layout 575 Kit Ap SW	
234536	DxDesigner 076 Bnd SW	
234351	PADS IO Designer Ap SW	
234352	PADS IOD PCB View Op SW	
234353	PADS IOD PCB Opt Op SW	

ANALYSIS & SIMULATION		AVAILABLE PLATFORMS
130009	Eldo Analog Design Stn SW	WIN
221154	Eldo for HyperLynx Op SW	
225414	HyperLynx Analog Op SW	
239985	HyperLynx SI GHz Bnd SW	
233857	HyperLynx Thermal Ap SW	
236251	EZwave for HyperLynx Ap SW	

PCB EXPEDITION

The Expedition Series flow is tailored for the mid to large-sized organization or the systems design group with pervasive use of leading edge PCB or high speed technologies. This tightly integrated solution composes the industry's most advanced design and analysis functionality in an environment of constraint, library and design data management.

- Most advanced place and rout technology for high design productivity, fast time-to-market and performance optimized products.
- High-speed pre and post-layout analysis for classical MHz routes and multi-gigabit serial interconnects.
- Design capability for leading PCB technologies such as HDI/ microvia, embedded components, flex and rigid –flex and high pin-count/performance IC packages.
- Tight integration with FPGA design solutions for reduced design cycle time and optimized system performance.
- Common constraint editing and management system feeds all tools in the flow for one-time, easy-to-use entry.
- Patented concurrent team design technology reduces layout design time by 40-70%.



The PCB Expedition package includes:

- Design Capture & System Design - DxDesigner Products
- PCB Layout – Expedition Pinnacle, Team PCB
- Manufacturing – CAM Output Manager, Fablink XE Pro
- Signal Integrity Analysis – HyperLynx GHz, Quiet Expert
- Board Level Simulation – HyperLynx
- FPGA Integration – I/O Designer
- Thermal Simulation – HyperLynx

PCB EXPEDITION TOOLS

SYSTEM DESIGN PRODUCTS		AVAILABLE PLATFORMS
221965	Variant Mgr Bnd SW	
220524	EDIF 200 Graphics I/F Op SW	
225311	Electrical CES Ap SW	Linux, WIN
219171	I/O Designer Ap SW	
238784	DxDesigner ExpPCB Bnd SW	
234107	DxD RF Design Op SW	

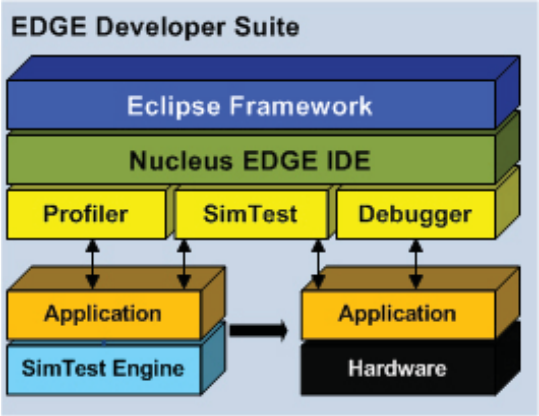
ANALYSIS & VERIFICATION PRODUCTS		
221154	Eldo for HyperLynx Op SW	
225414	HyperLynx Analog Op SW	
239985	HyperLynx SI GHz Bnd SW	
233857	HyperLynx Thermal Ap SW	Linux, WIN
220414	QUIET Expert Ap SW	
236251	EZwave for HyperLynx Ap SW	
239967	HyperLynx PI Power Bnd SW	

DATA MANAGEMENT PRODUCTS		
206071	Library Manager Ap SW	
206072	Parts Manager Admin Ap SW	Linux, WIN
206073	Parts Manager Client Ap SW	

PHYSICAL DESIGN PRODUCTS		AVAILABLE PLATFORMS
206143	Advanced Interconnect Op SW	
212132	Exp Design Reuse Op SW	
234108	ATP RF Design Op SW	
206079	Expedition PCB Browser Ap SW	
222402	Expedition PCB Pinnacle Ap SW	
220633	Fablink XE Pro Ap SW	
215981	OrCad schematic Exp IF Op SW	
225192	PCB DFF Analysis Op SW	Linux, SUN, WIN
206059	PCB Planner Ap SW	
206060	PCB Viewer Ap SW	
215737	TeamPCB - WG Op SW	
236799	3D PCB Viewer Op SW	
221242	ATP Flex for Expedition PCB Op SW	
227594	ATP Embedded Passives Op SW	

EMBEDDED SW DEVELOPMENT

Mentor Graphics' Embedded Software Development package provides a complete development, debug and testing environment for embedded software, including:



- Nucleus EDGE – An Integrated Development Environment (IDE) based on the industry-standard Eclipse framework. EDGE contains a powerful editor, a project manager, and build management facilities for a number of embedded toolsets.
- Nucleus Debugger – A source-level debugger supporting debugging operations on the ARM, MIPS, PowerPC, Nios II, and MicroBlaze platforms, as well as host-based debugging on Windows PCs. A number of advanced features are incorporated, including hardware-assisted feature support, codelet scripting support, SmartWatch tool tips, and I/O Channel support.
- Nucleus Profiler – An application to measure code-execution that plugs into the Nucleus EDGE environment. This allows developers to access hooks in the Nucleus RTOS to collect, measure, and display events through time.
- Nucleus Compiler Tools – An industry leading C/C++ compiler toolset supporting the widely used PowerPC architecture.
- Nucleus SIMdx - A development, execution and testing environment for embedded applications. Enables software integration, man-machine-interface and system level testing without hardware. Applications running under SIMdx are debugged with Nucleus Debugger.

EMBEDDED SW DEVELOPMENT TOOLS

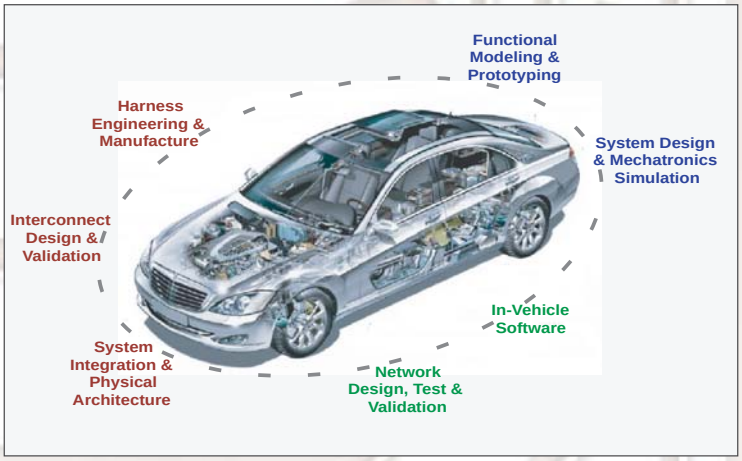
EMBEDDED SOFTWARE		AVAILABLE PLATFORMS
230918	EDGE Developer Suite ARM GNU Compiler Tools EDGE SimTest Microtec C Compiler PPC EDGE Debug EDGE Profiler	WXP

AUTOMOTIVE TOOLS

Over the last 20 years the number of mechatronic systems in the typical automobile has grown from an average of four to more than 20 and as many as 80. In response to the need for improved quality, efficiency and functionality of the design-to-manufacture flow while managing costs across the product life cycle, Mentor Graphics' solutions respond to the demanding problems of modern EE design.

Mentor Graphics offers design packages specifically for automotive engineering, comprising:

- Capital Harness Systems (CHS) – Electrical distribution system design, simulation and analysis, design data and change management, engineering and manufacturing analysis and support, enterprise integration (bridges for MCAD, PDM, etc.)
- Volcano™ Communication Technology – Network design automation tools, multiplex bus system analysis (CAN, LIN, FlexRay, etc.), deterministic approach to "correct-by-construction" in-vehicle software, network test and validation

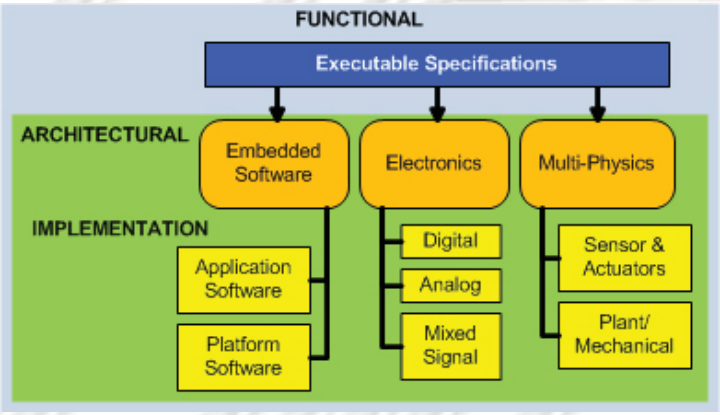


SYSTEM MODELING

System Vision - A complete environment for creation and verification of mixed-signal and multi-language systems using the power of VHDL-AMS to verify your control and mechatronic systems.

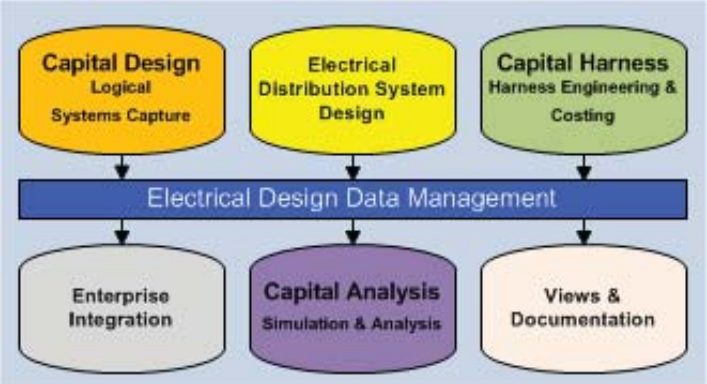
SystemVision targets the following applications:

- Automotive Electrical Systems, addressing challenges such as increased vehicle mechatronic content, dual voltage system architecture design, function design & analysis & communication systems.
- Control Systems, such as system concept feasibility, digital/analog subsystem partitioning, hardware/software/firmware partitioning, subsystem I/O specification & dynamic system interactions not found at the subsystem level.
- Mechatronic Systems Design technology challenges such as mixed-technology systemic interactions, device sizing & component rating & algorithm testing with "software in the loop" capabilities.



CABLING & HARNESS

Capital Harness Systems (CHS) - Addresses the complexities of integration and interconnection of electrical systems and design of their associated wire harnesses by providing a common, attractive user environment; a very rich data structure; and infrastructure services such as security and data reporting, and innovative functionality specialized to the electrical domain. This includes electrical distribution system design, simulation and analysis, design data and change management, engineering and manufacturing analysis and support, enterprise integration (bridges for MCAD, PDM, etc.).



Benefits

- Fully integrated application suite for electrical system design, electrical analysis, system integration / wiring design and harness engineering.
- Powerful embedded data management capabilities (vehicle configuration management, design comparison, data sharing etc).
- Productivity enhanced by modern technologies (wiring synthesis, interpretive analysis, diagram synthesis, etc).
- Architected for large organizations (multi-user, multi-site) with powerful enterprise integration capabilities.

CABLING & HARNESS TOOLS

CAPITAL HARNESS		AVAILABLE PLATFORMS
237294	CHS Integrator Comp Ap SW	Linux, SUN, HP, WIN
222413	CHS AVAssist Integrator Op SW	
223747	CHS Brg UG NX3 Int Elc Op SW	
222016	CHS Bridge UGS NX3 Elec Op SW	
221957	CHS Capital SimGrid Ap SW	
223381	CHS Ground Design Op SW	
223743	CHS Integration Server Ap SW	
234971	CHS Ent Reporter Ap SW	
222581	CHS Logic Ap SW	
240873	CHS Topology Op SW	

CAPITAL HARNESS		AVAILABLE PLATFORMS
221984	CHS SimCertify Op SW	Linux, SUN, HP, WIN
221985	CHS SimProve Op SW	
221986	CHS SimScript Op SW	
221960	CHS SimStress Op SW	
233365	CHS SimBridge Op SW	
237474	CHS HarnessXC Adv Bnd SW	
VESYS 2.0 PRODUCTS		
226551	VeSys Electrical Bnd SW	WIN
SYSTEMVISION PRODUCTS		
238218	SystemVision 650 Bnd SW	WIN

VEHICLE NETWORKING

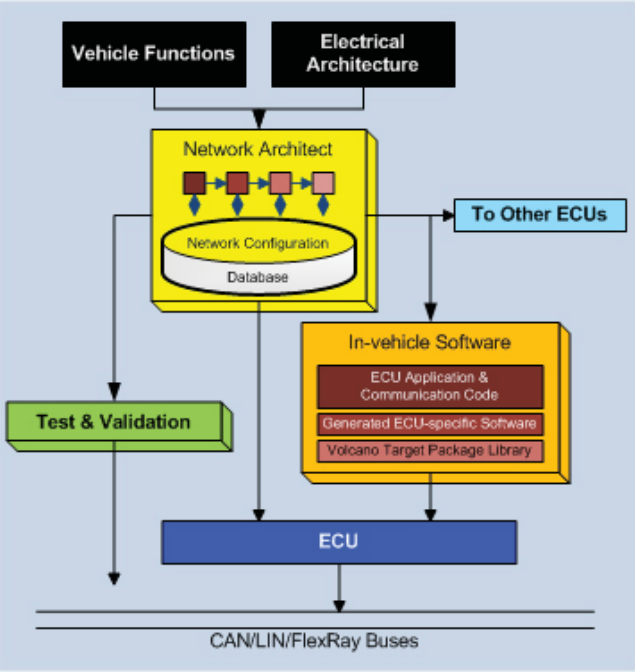
Volcano Network Architect (VNA) is Mentor Graphics' design and analysis tool for CAN and LIN communication systems. VNA provides design, analysis and administrative functions and supports designing systems with legacy electronic control units (ECUs) with fixed messaging. VNA is a standalone tool suitable for integration in legacy design processes as well as the ideal foundation for building a system engineering-based communication design process on. The VNA connects easily to other tools, for example enterprise-wide communication databases.

Volcano Network Architect: High level requirement capturing early in the design, automatically map signals to frames for better bandwidth utilization. HW-independent, signal-based API abstracting.

Volcano In-Vehicle Software: Signals-oriented API simplifies application development by abstracting the communication from the application; predictable behavior reduces testing.

Volcano Test and Validation: Monitor and display multiple network signals in one tool. Advanced emulation capabilities for simulating user-defined functionality.

System Vision: A mixed-signal modeling & simulation environment using the power of VHDL-AMS to verify your control & mechatronic systems.



VEHICLE NETWORKING TOOLS

VEHICLE NETWORKING		AVAILABLE PLATFORMS
225668	Volcano VNA Integrator Seat	
225667	Volcano VNA Data Server Lic	WIN
225670	Volcano LNA Dev Seat License	
SYSTEM VISION		
238218	SystemVision 650 Bnd SW	WIN

MECHANICAL ANALYSIS

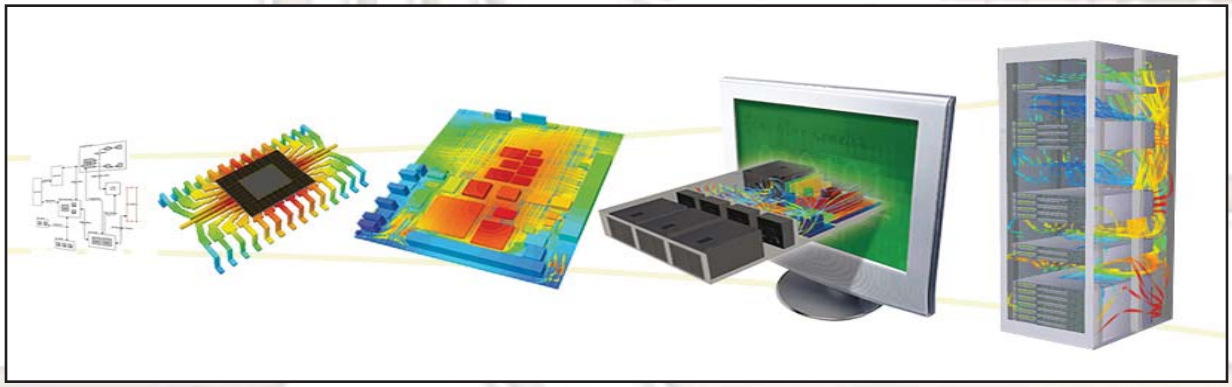
Mentor Graphics Higher Education Program's Mechanical Analysis Package provides complete solutions for electronics thermal design (electronics cooling); building heating and ventilation (HVAC); and Concurrent CFD – Computational Fluid Dynamics software embedded in a mechanical CAD environment.

Electronics Thermal Design - Mentor Graphics supports the complete thermal design of electronics from IC package through to system-level cooling.

- **FloTHERM™** - 3D computational fluid dynamics software that predicts airflow and heat transfer in and around electronic equipment, from components up to complete systems.
- **FloTHERM PCB™** - accelerates the conceptual thermal design of printed-circuit boards.
- **FloTHERM PACK™** is a Web-based solution that generates accurate thermal models of IC components, test boards, test harnesses and other associated parts with minimum effort.

Building Heating & Ventilation - FloVENT™ predicts and optimizes airflow & quality, temperature and contamination control in all types of buildings from data IT rooms, clean rooms, auditoriums, office buildings, car parks, vehicles, laboratories & hospitals.

Concurrent CFD - helps Engineers overcome challenges with Mechanical Engineering projects. **FloEFD™** is a full-featured 3D fluid flow and heat transfer analysis package without the numerical complexity and meshing overhead of traditional CFD.



MECHANICAL ANALYSIS TOOLS

MECHANICAL ANALYSIS		AVAILABLE PLATFORMS
239801	FloTHERM Ap SW	Linux, SUN, WIN
239808	FloTHERM Parallel Ap SW	
239804	FloTHERM Solver Op SW	
239803	FloTHERM 4 CC Solver Op SW	
239805	FloTHERM Parallel Solver Op SW	
239806	FloTHERM 4 CC Parallel Solver	
240109	FloTHERM.PCB Ap SW	
238133	FloTHERM.PACK Subscription	
239822	FloMCAD.Bridge Ap SW	WIN

MECHANICAL ANALYSIS		AVAILABLE PLATFORMS
239811	FloVENT Ap SW	SUN, WIN
239815	FloVENT Parallel Ap SW	
239817	FloVENT Solver Op SW	
239816	FloVENT 4 CC Solver Op SW	
239818	FloVENT Parallel Solver Op SW	
239819	FloVENT 4 CC Parallel Solver Op SW	
238141	FloEFD Ap SW	WIN
238154	FloEFD Electronics Cooling Op SW	
238395	FloEFD Adv CFD Module Op SW	

RENEWING MEMBERS ONLY

For our existing members, please make sure that you that you review this section as it contains information on the changes to this years program and packages available only to members renewing the use of specific tools.

This year, notable modifications to our product collection are as follows:

IC NANOMETER DESIGN

New Products

- ADiT Rail, Calibre nmDP-C, Calibre Metrology are now available

Removed Products

- HP-GL and HP-GL/2 Filters are no longer available. Printing functionality is available within the IC Station products

DESIGN, VERIFICATION & TEST

Silicon Test Products

- MBISTArchitect and BSDArchitect have been replaced by Tessent MemoryBIST and Tessent BoundaryScan
- DFTAdvisor has been replaced by Tessent SoCScan, though all functionality is included in the new tool
- FlexTest is no longer available

Functional Verification Products

- CDC Compiler and FV Eng are replaced by new products CDC Ap SW and Formal Ap SW
- The Questa MVC Library is now available

PCB EXPEDITION

New Products

- HyperLynx PI (Power Integrity Analysis) is now available
- DxDesigner RF Design is now available

Cabling & Harness

New Products

- CHS Topology is now available

RENEWING MEMBERS ONLY

PACKAGES AVAILABLE FOR RENEWING MEMBERS ONLY

The following two packages, PCB Expedition Renewals and PCB Board Station are only available to members who are renewing the use of these tools.

PCB EXPEDITION RENEWALS

	COMPONENTS	AVAILABLE PLATFORMS
206052	Design Capture Ap SW	L, WIN
206068	Design Capture PI Ap SW	
206050	DesignView Ap SW	
215729	Spice Integration Op SW	
056401	FlowXpert Ap SW	Linux, HP, WIN
056403	ProjectXpert Ap SW	
056402	XpertBuilder Ap SW	

	COMPONENTS	AVAILABLE PLATFORMS
204418	IS Synthesizer Ap SW	Linux, SUN, HP, WIN
204422	IS_Analyzer Ap SW	
204419	IS FloorPlanner Ap SW	
204420	IS Optimizer Ap SW	
204417	IS MultiBoard Op SW	
206069	EDIF 2.0.0 Schematic I/F Ap	Linux, SUN, WIN
221331	TAU Ap SW	

PCB BOARDSTATION

	COMPONENTS	AVAILABLE PLATFORMS
062000	Board Architect Stn V8 SW	Linux, SUN, HP, WIN
039986	Board Stn V8 SW	
044164	MultiChipMod Dsnr Stn V8 SW	
034640	ProtoView V8 Ap SW	
057119	EngineerView Lite V8 Op SW	
057123	Hispeed Lite V8 Op SW	
057105	ManufactureView V8 Ap SW	
034635	PCB PACKAGE V8 Ap SW	
051637	Interactive Layout V8 Ap SW	
042732	PCB Mechanical I/F V8 Op SW	
051576	PTM:SITE V8 Op SW	
034625	AutoTherm V8 Ap SW	
067977	RF Architect V8 Op SW	
067978	RF Layout V8 Op SW	
202131	RF EM Sim Interface Op SW	
204418	IS Synthesizer Ap SW	
204422	IS_Analyzer Ap SW	
204419	IS FloorPlanner Ap SW	
204420	IS Optimizer Ap SW	
204417	IS MultiBoard Op SW	
221331	TAU Ap SW	
206644	RE AutoRouter V8 Op SW	
056401	FlowXpert Ap SW	SUN, HP, WIN
056403	ProjectXpert Ap SW	
056402	XpertBuilder Ap SW	
051640	Falcon ITK V8 Ap SW	

	COMPONENTS	AVAILABLE PLATFORMS
217332	EDIF 200 Netlist Reader Op SW	Linux, SUN, HP, WIN
218751	EDIF 200 Schm Reader Op SW	
218753	EDIF 200 Schm Writer Op SW	
218752	EDIF 300-400 Schm Reader Op SW	
218755	EDIF 300-400 Schm Writer Op SW	
218756	EDIF 300-400 Netlist Reader Op SW	
205653	HDLWrite PLUS V8 Ap SW	
054804	HP Hp-GL Filter V8 Ap SW	
054805	HP HP-GL/2 Filter V8 Ap SW	
054806	Postscript Filter V8 Ap SW	
054769	Schematic Generator V8 Ap SW	
206644	RE AutoRouter V8 Op SW	
206646	RE Network AutoRouter V8 Op SW	
206645	RE HighSpeed V8 Op SW	
215736	TeamPCB - EN Op SW	
030000	Falcon Framework V8 Ap SW	
203465	Continuum QS Stn SW	
051630	HDL-A/DEV V8 Op SW	
220391	Idea StationII SW	
217771	BPL-CAD Lib V8 Op SW-LSL10	
59834	BPL-Dig Analysis V8 Op SW-SL	
034649	QuickFault II Kernal V8 Op SW	

SUPPORT, TRAINING & MEMBERSHIP

SUPPORT

As a member of the Higher Education Program you are entitled to the same customer support services as standard Mentor Graphics customers. SupportNet, www.mentor.com/supportnet, Mentor's online support, provides the fastest and easiest way to resolve your technical and licensing support issues:

- SupportNet KnowledgeBase - an intelligent online query database to access technical notes and solutions to previously addressed solutions.
- Download of Product Updates and Patches for all Mentor Graphics products, to bring you the latest improvements in product functionality, usability and performance.
- Service Requests - logging of technical and licensing support requests, which are handled with exactly the same priority as phone support. You can often provide more information using online requests (such as error transcripts) to help the support engineer resolve your problem faster. You may also track your service requests whether logged online or by telephone.

SupportNet Registration only takes a few minutes (you will need your Mentor Graphics Site Number). Access is immediate (72 hours access granted pending registration confirmation).

The only 5 time recipient of the Software Technical Assistance Recognition (STAR) Award in EDA for technical support excellence.

The only EDA support provider with global support center practices certified by the Support Center Practices (SCP)

TRAINING

Mentor Graphics offers a wide range of classes and web-based events and is committed to ensuring that members are fully trained in the use of Mentor's tools. In North America and Europe, faculty and teaching staff members are eligible to attend Mentor Graphics' advertised public training classes at zero cost on a space available basis. To view or register for these courses, visit the Education Services Website, www.mentor.com/training_and_services.

For other regions, please contact your local HEP representative.

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Mentor Graphics partners with CMC Microsystems to donate our design tools to CMC member universities.

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Fax: (613) 548-8104
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Mentor Graphics also partners with EUROPRACTICE to donate tools to Universities.

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